MIXED BASEBAND-IF PREDISTORTION SYSTEM FOR LINEARISING POWER AMPLIFIERS

TECHNICAL FIELD

The present patent request for industrial invention concerns a mixed baseband-IF predistortion system which linearises amplifiers that exhibit non linear distortion phenomena.

BACKGROUND OF THE INVENTION

Usually an instantaneous non linear amplifier can be modelled by its AM/AM and AM/PM distortion curves [1], [2]. Both types of non linear distortions produce the spectral regrowth of the amplifier output; this spectral regrowth can be classified in the two following categories:

- In band intermodulations
- Out band intermodulations.

The firsts cannot be eliminated by linear filtering and they are responsible for the signal-to-noise ratio degradation and, consequently, for the Bit Error Rate (BER) degradation in digital communication systems. The seconds generate the interference between adjacent channels and they can be filtered out at the amplifier output with a certain output power penalty that is caused by the filter insertion losses.

Baseband predistortion is one of the known techniques to counteract for AM/AM and AM/PM distortions [2][3] and its digital adaptive implementation was widely investigated in the last years [4] [5] [6] [7].

The IF predistortion is another well known technique to compensate for AM/AM and AM/PM non linearities [8],[9],[10]. The IF predistortion technique distorts the instantaneous amplitude of a real signal that has been generated by the modulation of a complex baseband signal up to an intermediate frequency (IF) that lies between the baseband frequency and the transmission radio frequency (RF).

On the contrary Baseband Predistortion works directly on the complex baseband signal and it distorts its instantaneous envelope.

The theoretical equivalence of the two techniques and the analytical relation between them are known in the literature [2].

These techniques are different, instead, from the technological point of view: indeed, the baseband predistortion generally uses digital technology, while the IF predistortion take advantage of analogue devices, with a consequent limited precision in the precorrection strategy.

Nevertheless, it may be theoretically possible to think to realise an IF predistorter that employs only digital technology. This approach would require the use of digital components that must be capable to work at sampling frequencies higher than those that are required by an equivalent baseband predistorter.

Consequently it is not generally advantageous, if not even technologically impossible, to realise an IF predistorter that is completely digital and capable of working on large bandwidth signals.

At the same time, however, the realisation of an IF predistorter, which would be characterised by a precorrection accuracy that is equal to the one guaranteed by its digital baseband implementation, should be preferred to that of a baseband predistorter when such a predistorter should replace old analogical IF predistorter that are employed in already existent transmission systems.

Indeed, in such a case, the replacement of the old predistorter would not modify the overall transmitter architecture, differently from what would happen with a baseband predistorter, with advantages that are evident both in terms of maintenance costs and designing time.

No one of the already known predistortion schemes propose mixed solutions for baseband and IF predistortion strategy.

Another aspect that has to be highlighted is the fact that even an ideally predistorted amplifier (both by baseband or IF predistortion) can be modelled as a device, which in the following will be called soft-limiter, that limits the signal envelope to be lower than a certain maximum value.
As a consequence the saturation non linear distortion is not avoidable every time that the signal modulation is characterised by a non constant envelope and the amplifier doesn't work with an adequate difference between the maximum and the mean output power. This situation is typical for multicarrier signals that are characterised by an high peak-to-mean power ratio; consequently, their maximum signal envelope is usually reduced by an operation, that it is called clipping, in order to have a more efficient power amplification even if paying the price of a reduced spectral purity. The difference between the maximum and the working amplifier output power is commonly said the back-off.
One object of the present invention is to realise a predistortion system to linearise amplifiers, working on signals that are modulated at an intermediate frequency IF, but exploiting the precorrection accuracy that is typical of the digital implementations.
The invention consists exactly in the realisation of a device that, by exploiting the baseband representation of the input signal, should be capable to calculate the amplitude and the phase predistortion that are necessary to linearise a non linear amplifier by a baseband digital device, and that implements at IF the said predistortion by using analogical devices.
The said objective is reached, by means of what has been discovered, by a baseband digital system that includes at least a circuit for the predistortion computing, a digital delay line and a Digital-to-Analog converter and by an analogical system that modifies the gain and the phase of the IF modulated input signal as a function of the output of the said baseband digital system.
This solution allows reducing the complexity of a completely digital implementation of the IF predistorter, even if maintaining almost the same predistortion quality of a baseband predistorter that is completely digital.
Other object of the present invention is to realise a predistortion system to make cheaper and less complex, or even to eliminate, the amplifier output filters that are used to reduce the out band spectral regrowth.
The said objective is achieved, by means of what has been discovered, by including in the predistortion system also a pre-clipping circuit and at least a filter that eliminates the out band spectral regrowth. The pre-clipping term is used to remark that the clipping operation has to be performed before the predistorting one.
Another aim of the invention is to provide adaptation to the predistortion system.
This objective is achieved, by means of what has been discovered, by including in the predistortion system both an input-output error circuit that provides the values to modify the action of the said predistortion circuit and a timing circuit to synchronise the input to the output of the system.
Some considerations are reported in the following to better understand the reasons to introduce the clipping before the predistortion circuit:

- Both the predistortion circuit and the RF amplifier introduce non linear distortions (i.e. AM/AM and AM/PM) that only depend on the baseband signal envelope and, consequently, on the instantaneous signal power.
- The ideal combination of the predistortion circuit with the amplifier gives rise to an overall system that is characterised by a completely cancelled AM/PM curve and by a residual AM/AM curve that acts as a soft limiter of the baseband signal envelope.

This means that the RF output of the ideally predistorted amplifier is equivalent to the RF modulation of a complex baseband signal whose envelope is passed through a soft limiter device. The residual distortion introduced by the soft limiter depends on the signal peak-to-mean power ratio and on the input back off to the predistorted system (soft limiter).
A residual distortion is introduced every time the input back off to the predistorted system is lower than the peak-to-mean power ratio of the signal.

The distortions become as more evident as the input signal is characterised by a high peak-to-mean power ratio.
If the predistorted amplifier introduces some clipping on the signal envelope, the consequent spectral regrowth will degrade the signal with respect to the signal-to-noise ratio and the adjacent channel interference.
The signal-to-noise ratio degradation for a fixed input back off is not avoidable because it depends on the in band intermodulations. On the contrary, the linear filtering of the out band intermodulations that are produced by the clipping can reduce the adjacent channel interferences.
If the predistorted amplifier generates some clipping, the only way to reduce the adjacent channel interference is to introduce a RF filter at the amplifier output.
The consequence is a significant expense in terms of equipment costs and a reduction of the available output power because of the filter insertion losses.
An idea that characterises this invention is to realise at baseband a clipping on the signal envelope that is analogous to the one that would be introduced by the predistorted amplifier.
Such an approach allows, by the use of devices that in the following we will call post-clipping filters, a baseband counteraction of the adjacent channel interference that are introduced by the clipping circuit itself.
In this way it is possible to obtain the same residual adjacent channel interference, for a given output power, that would be obtained by using RF selective filters, with a significant reduction of the system costs.
However both the clipping and the post-clipping filtering has to be implemented before the predistortion circuit, in order to not vanish the predistorter action.
In this way, the output of the post-clipping filters represents the baseband equivalent of the best residual distorted signal that can be obtained at the predistorted amplifier output.
In order to clarify the notation that will be used in the following of the description and in the included figures we remind that an RF signal $x(t)$, that is modulated at an RF frequency $f_o = \frac{\omega_o}{2\pi}$ can be analytically represented by the following expression

$$x(t) = R_x(t)\cos\{\omega_o t + \theta_x(t)\}$$

where $R_x(t)$ and $\theta_x(t)$ respectively represent the instantaneous envelope and the instantaneous phase of the modulating signal.
The signal can be equivalently represented at baseband by the complex signal $\hat{x}(t)$ that is defined in polar notation as

$$\hat{x}(t) = R_x(t)\cdot e^{j\theta_x(t)}$$

The complex signal $\hat{x}(t)$ can be also represented by its cartesian notation as

$$\hat{x}(t) = x_I(t) + jx_Q(t)$$

where $x_I(t)$ and $x_Q(t)$ are respectively the so called In-phase and Quadrature signal components and they are related to the polar notation by the following expressions

$$x_I(t) = R_x(t)\cdot\cos\left[\theta_x(t)\right]$$
$$x_Q(t) = R_x(t)\cdot sen\left[\theta_x(t)\right]$$

The relationship between the signal $x_{RF}(t)$, which is modulated at a frequency $f_{RF} = \frac{\omega_{RF}}{2\pi}$ and its complex baseband equivalent is expressed by the following analytical expression

$$x_{RF}(t) = \mathrm{Re}\left\{\hat{x}(t)\cdot e^{j\omega_{RF}t}\right\} = x_I(t)\cos(\omega_{RF}t) - x_Q(t)\sin(\omega_{RF}t)$$

The system architecture of a possible, but not limiting, realisation of a predistortion system that exploits the invention will be described in the following making use of the complex signal representation and taking advantage of the included figures from 1 to 7.
The Fig.1 shows the scheme of an amplification system that employs a mixed baseband-IF Predistortion System (1), which considers the use of a Clipping & Interpolation Circuit (4), of a Predistortion Computing Circuit (2) and of an IF Predistortion Actuating Circuit (3) that works at a frequency $f_{IF} = \omega_{IF}/2\pi$ that lies between the baseband and the transmitting frequency $f_{RF} = \omega_{RF}/2\pi$ at which the amplifier works.
The depicted scheme is redundant. Indeed, even only one of the two Predistortion Computing Circuit (2) inputs is sufficient in order to make the system working.
Moreover also the Clipping & Interpolation Circuit (4) could be eliminated if the input signal $\hat{x}(t)$ does not need such processing or in the case it is not of interest to exploits the potentiality of combining the clipping action with the predistortion action.
The Fig.2(a) shows with greater detail the Clipping & Interpolation Circuit (4) scheme that is positioned before the Predistortion Computing Circuit (2).
In this case the Interpolation Circuit (5) stays before the Clipping Circuit (6).

Specifically the Interpolation Circuit (5) can be realised by a Filling Circuit (5a) that inserts (N-1) zeros, or (N-1) replica of each sample, between the signal input sample, with N being the interpolation factor. The real interpolation function is performed in cascade by the action of the Interpolation Filter Circuit (IFC) (5b).
The signal that has been interpolated in such a way is elaborated by the Clipping Circuit (6) which firstly limits its maximum envelope (by the Clipping Device (6a)) and afterward eliminates the out band spectral regrowth (by the Post Clipping Filters Circuit (PCF) (6b)).

Instead, the Fig.2(b) represents the a Clipping & Interpolation Circuit (4) that is alternative to that of Fig.2(a).
In this case a Clipping & Interpolation Circuit (4) firstly performs the Clipping action by the Clipping Device (6a), which is followed in cascade from the Filling Circuit (5a) that introduces some zeros or some input sample replica. The Filling Circuit (5a) is followed by the Filtering Circuit (5c) that jointly realises the real interpolation filtering (IFC) and the post clipping filtering (PCF) of the signal outband spectral regrowth.

The Fig.3(a) and 3(b) graphically show the clipping operation that is performed on two general complex signals $V_{1,2} = V_{I_{1,2}} + jV_{Q_{1,2}}$ by the Clipping Device (5a).
The Fig.3(b) and 3(a) respectively represent the action of a Cartesian Clipping Device and the action of an Envelope Clipping Device. The first separately cuts each one of the (V_I, V_Q) components that overcomes a certain value, while the second jointly works on the (V_I, V_Q) components by cutting them in such a way that the envelope is lower than a certain threshold.
The Fig.4 shows a possible realisation scheme for the baseband Predistortion Computing Circuit (2). This scheme considers to employ a circuit that extracts the input signal envelope.
The input $s(t)$ can be a baseband signal and consequently it can be represented by means of the complex notation as $s(t) = s_I(t) + js_Q(t)$. The input signal $s(t)$ may also be modulated at a frequency f_{IF} and it may be expressed by the relation
$s_{IF}(t) = s_I(t)\cos(2\pi f_{IF}t) - s_Q(t)\sin(2\pi f_{IF}t)$.
In the first case the envelope $R_s(t)$ of such a signal is extracted by a baseband Envelope Detector (2f) that performs the analytical operation that is expressed by the relation $R_s(t) = \sqrt{s_I^2(t) + s_Q^2(t)}$.

In the second case the signal envelope is extracted by an IF Envelope Detector (2g) that could be realised by analogical components likewise a classical envelope demodulator.
In the case that the Predistortion System (1) wants to consider both the options, the Predistortion Computing Circuit (2) has to include both the Circuit (2f) and the Circuit (2g) as well as an Input Selector (2i).
The Circuit (2) considers that the input signal envelope R_s would be in digital format. In the case that the input signal $c(t)$ is not already digital, it can be converted in digital format by the Analog-to-Digital Converters (2e)(2h) that differently would not be present. The R_c envelope represents the signal by which the Predistortion Table (7) is addressed.
The Predistortion Table (7) is organised in two Tables (7a) and (7b) in which are stored the values that respectively determine the non linear gain (g or G) and the non linear phase (ϕ or Φ) of the IF Actuation Circuit (3).
The Circuit (2a), (2b) and (2c) has the only roles to opportunely delay the Table (7) output control signals, to convert them in analogical format and to adapt their dynamic to those of the IF Actuation Circuit (3) controls.
Two equivalent solutions to realise the IF Predistortion Actuation Circuit (3) are shown in Fig.5(a) and 5(b).
The Fig.5(a) scheme considers that the Gain Actuator (3a) stays before the Phase Actuator (3b), while the two actuators invert their position in the Fig.5(b) scheme. The two analogical actuators are designed in such a way that one realises a phase modulation while the other realises an amplitude modulation, generating in this way the signals that are shown in Fig.(5a) and (5b) whose analytical expression are reported in the following:

$$s_{IF}(t) = R_S(t)\cos\left[\omega_{IF}t + \theta_S(t)\right]$$

$$y_{IF}(t) = G\left[R_S(t)\right]\cdot R_S(t)\cdot\cos\left[\omega_{IF}t + \theta_S(t)\right]$$

$$w_{IF}(t) = R_S(t)\cdot\cos\left[\omega_{IF}t + \theta_S(t) + \Phi\left[R_S(t)\right]\right]$$

$$z_{IF}(t) = R_S(t)\cdot G\left[R_S(t)\right]\cos\left[\omega_{IF}t + \theta_S(t) + \Phi\left[R_S(t)\right]\right]$$

The Fig.6 shows the scheme of an amplification system that includes the adaptation of the mixed baseband-IF Predistortion System (1).
This scheme includes the use of a Synchronisation Circuit (8) for the synchronisation of the Predistortion Computing Circuit (3) input signal $\hat{s}(t)$ with the RF amplifier output signal $\hat{a}(t)$.
A circuit (9) is also employed in order to determine the input-output error signal.
The Fig.7 represents the logical scheme of a potential realisation of the Error Circuit (9)

The signal $\hat{x}(t)$ in Fig.1 represents a complex digital signal at the input to the Predistortion System (1). This signal $\hat{x}(t)$, after its conversion in digital format by Analog-to-Digital converters, can be eventually oversampled by the Interpolation Circuit (5) of Fig.2(a) or by the Circuit (5a) of Fig.2(b), if the input sample frequency is not high enough to correctly represent it in a non linear environment.
The Clipping Device (6a) that is shown Fig.2(a) or Fig.2(b) limits the peak-to-mean power ratio of the signal in order to avoid or reduce any other clipping or saturation phenomenon that could be introduced by the Predistortion Actuating Circuit (3) and/or the RF Amplifier.

The Clipping Device (6a) reduces the signal peak-to-mean power ratio constraining the envelope of the baseband signal inside a circle of the complex plane, as shown in Fig.3(a), by a technique that is called Envelope Clipping.

It is possible, anyway, to reduce the peak-to-mean power ratio also by using some others clipping strategies. An alternative choice, for example, is to separately clip the In Phase and In Quadrature signal components as shown in Fig.3(b), by a technique that is called Cartesian Clipping. The Cartesian Clipping reduces the signal envelope but it also introduces some extra phase distortion on the signal as shown in Fig.3(b).
Moreover the Cartesian Clipping is not exactly matched to the Envelope Clipping that is introduced by the predistorted amplifier. As a consequence the predistorted amplifier will introduce further clipping if the complex signal clipping is realised outside to the square that is circumscribed to the amplifier clipping circle. On the contrary, unneeded extra distortions is introduced by the Cartesian Clipping if the clipping square is inscribed into the amplifier clipping circle, as shown in Fig.3(b).
However the Cartesian Clipping is easier and cheaper to implement and consequently it may be considered as a good compromise between performance and costs.
Any kind of clipping strategy can be performed before or after the interpolation process (see Fig.2(a) and Fig.2(b)) if the Interpolation Circuit (5) is included in the Predistortion System (1).
The Clipping Circuit (6) that is placed after the interpolation circuit represents the best solution in terms of the achievable performance.
The other approach, nevertheless, is characterised by a lower system complexity because the Post Clipping Filters Circuit (6b) acts as the interpolation filter also.
The output $\hat{s}(t)$ of the Clipping & Interpolation Circuit (4) and its counterpart $s_{IF}(t)$ at the output of the Quadrature Modulator (10) represent the input for the Predistortion Computing Circuit (2) and for the IF Predistortion Actuating Circuit (3) respectively.
The Predistortion Computing Circuit (2) that is shown in Fig.4 employs the envelope $R_s(t)$ that is extracted from the input signal for addressing the Predistortion Table (7) in order to generate two baseband signals $G\left[R_s(t)\right]$ and $\Phi\left[R_s(t)\right]$, which would control the operation of the IF Predistortion Actuating Circuit (3).
The IF Predistortion Actuating Circuit (3) of Fig.5(a) or Fig.5(b) use the control signals $G\left[R_s(t)\right]$ and $\Phi\left[R_s(t)\right]$ to realise an amplitude and a phase modulation of the IF clipped signal $s_{IF}(t)$ by respectively employing the Gain Actuator (3a) and the Phase Actuator (3b).
The control signals at the Tables (7a) and (7b) output are opportunely delayed by using the Digital Delay Lines (2a) in such a way to synchronise them self to the IF signals that they are going to modulate.
The signals at the Digital Delay Lines (2a) output are reconverted in analogical format by Digital-to-Analog Converters (2b) and successively they are adapted to the control dynamic of their respective IF Actuators (3a) and (3b) by using the Dynamic Converters (2c), which realise a conversion of the control signal by means of input-output relationships of the kind

$$y_{out} = a \cdot y_{in} + b$$

in which ‘a’ and ‘b’ are two opportune constants.
Moreover, the two IF Actuator (3a) and (3b) can interchange their position inside the Predistortion Actuating Circuit (3) without altering the predistortion strategy.
The two non linear function ‘g’ and ‘ϕ’ that are stored in the Predistortion Tables (7) must be chosen in such a way that IF Predistortion Actuating Circuit (3) will generate distortions that compensate the ones that are introduced by the amplifier.
Furthermore, these distortions must be different from those that are required to compensate only the amplifier AM/AM and AM/PM curves in such a way that they could also compensate the eventual non linear behaviour of the analogical Actuator (3a) and (3b) and/or the non linear characteristic of the IF Envelope Detector (2g).

The Predistortion Computing Circuit (2) can also adapt the distortion that it introduces, according to the changes that are caused by the amplifier ageing, the temperature variations, the channel or the power switching and so on.
The Error Circuit (9) has the role to estimate the input-output non-linear error of the predistorted system and to provide an error signal $\hat{e}(t)$ to the Predistortion Computing Circuit (2).

The Error Circuit (9) can be realised in different ways and the Fig.6 shows one possible implementation of the error circuit, where the envelope (a scaled replica) and the phase of the Predistortion Computing Circuit (2) input $\hat{s}(t)$ are subtracted from the correspondent amplifier output $\hat{a}(t)$.

The two error signals $R_e(t)$ and $\theta_e(t)$ that are obtained in this way are subsequently weighted by two real coefficients α_R and α_θ in order to provide the correcting terms for the values that are stored in the Tables (7a) and (7b), which are responsible for the predistortion that is introduced by the Circuit (3).
The two error signals are analytically expressed by

$$R_e = \alpha_R \cdot [R_a - K \cdot R_d]$$

$$\theta_e = \alpha_\theta \cdot [\theta_a - \theta_d]$$

where K represents the desired linear gain for the predistorted amplifier.
The magnitude of the adaptation coefficients α_R and α_θ has to be chosen as a compromise between adaptation speed and noise rejection. The Synchronisation Circuit (8) has the role to estimate the loop delay of the adaptive system and to compensate it, in order to allow the Error Circuit (9) to correctly compare the input $\hat{s}(t)$ of the Predistortion Computing Circuit (2) with the amplifier output $\hat{a}(t)$.

We claim:

1. A mixed baseband-IF predistortion system for amplifiers linearisation, that is characterised by at least an IF predistortion actuating circuit (3) and by at least a baseband predistortion computing circuit (2) that controls the said circuit (3).
2. According to claim 1, a system that is characterised by the fact of including at least a clipping circuit (6) that is composed by a clipping device (6a) that is followed by at least a post-clipping filter (6b) or (5c).
3. According to claim 1, a system that is characterised by the fact that the said baseband predistortion computing circuit (2) includes at least: a table (7) in which storing the curves that allow the predistortion, a digital delay line (2a) and a digital-to-analog converter (2b).
4. According to claim 3, a system that is characterised by the fact that the said predistortion computing circuit (2) includes or takes advantage of a circuit for the envelope detection (2f) or (2g) to address the said table (7).
5. According to claim 3, a system that is characterised by the fact that the said predistortion computing circuit (2) address the said table (7) by the baseband cartesian components of the input signal.
6. According to claim 1, a system that is characterised by the fact that the said IF predistortion actuating circuit (3) distorts the IF modulated input signal by at least one control signal that is provided by the said baseband predistortion computing circuit (2).
7. According to claim 3,4,5, and 6, a system that is characterised by the fact that the output signal of the said predistortion computing circuit (2) is made by the said table (7) outputs, after they

have been converted in analogical format by the said digital-to analog converters (2b) and after they have been appropriately scaled by the dynamic converting circuits (2c).

8. According to claim 6, a system that is characterised by the fact that the said IF predistortion actuating circuit (3) is composed by the cascade of a gain actuator (3a) and by a phase actuator (3b), which modulate respectively the amplitude and the phase of the IF input signal by using two signals that are provided by the said baseband predistortion computing circuit (2).
9. According to claim 1, a system that is characterised by the fact of employing a circuit (5) for the interpolation of the input signal.
10. According to claim 9, a system that is characterised by the fact that said interpolation circuit (5) includes a device (5a) that introduces zeros, or replica of the first sample, between successive samples of the input signal, with the device (5a) that is followed by the interpolation filters circuit (5b) or (5c).
11. According to claim 2 and 9, a system that is characterised by the fact that, in the said clipping circuit (6), the clipping device (6a) is positioned before the said interpolation circuit (5) and in which the said post-clipping filters (5c) act as interpolation filters also.
12. According to claim 1, a system that is characterised by the fact of employing an error computing circuit (9) that generates at least one signal to modify the distorting action that is introduced on the said control signals of the said predistortion computing circuit (2).
13. According to claim 2 and 3, a system that is characterised by the fact that the said clipping circuit (6) is positioned before both the predistortion computing circuit (2) and the IF predistortion actuating circuit (3).
14. According to claim 2, a system that is characterised by the fact that the clipping device (6a) limits the input signal envelope without distorting its phase
15. According to claim 2, a system that is characterised by the fact that the clipping device (6a) separately limits the cartesian components of the input signal, thus distorting both the envelope and the phase.
16. According to claim 12, a system that is characterised by the fact that the said error computing circuit (9) generates the said error signals by the subtraction of the envelope and the phase of the amplifier baseband output signal from the corresponding components, at most scaled by a multiplication coefficient, at the input to the said predistortion computing circuit (2).
17. According to claim 16, a system that is characterised by the fact that each of the said error signals is multiplied by at least one weighting coefficient
18. According to claim 3,12 e 16, a system that is characterised by the fact of employing the said error signal to update the content of the said predistortion table (7)
19. According to claim 18, a system that is characterised by the fact that each value of the said predistortion table (7) of the said predistortion computing circuit (2), is updated, for each value of its address, by summing to its original content the value of the said error signal or a temporal mean that is performed on a number of values, that is greater or equal to one, that are consecutively assumed by the said error signal for each address value.

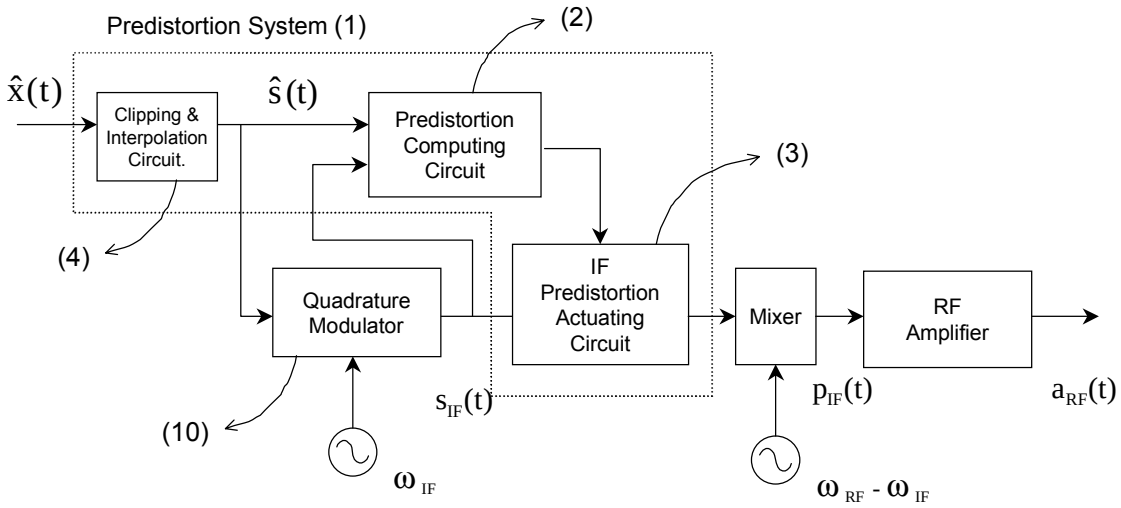


Fig.1

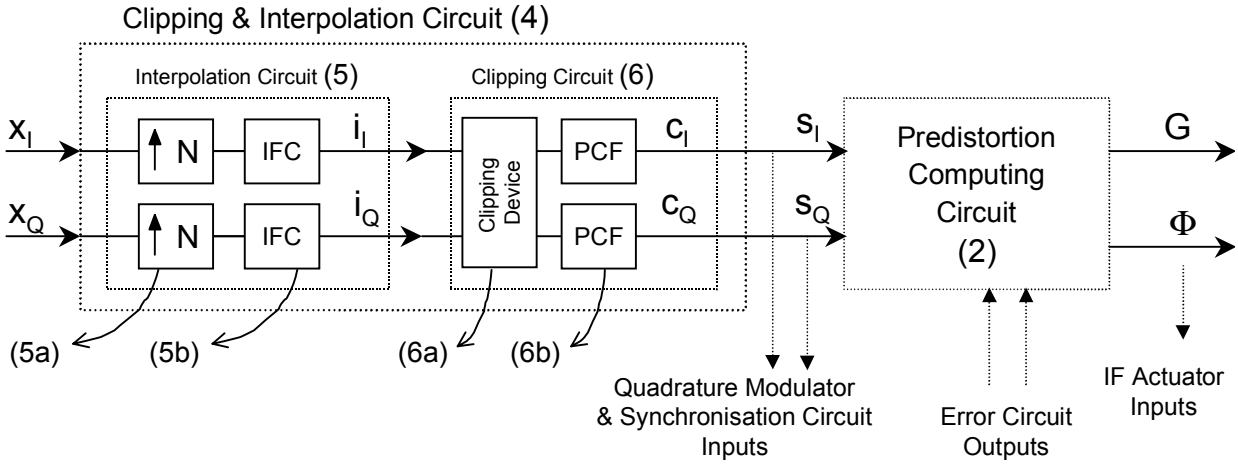


Fig 2(a)

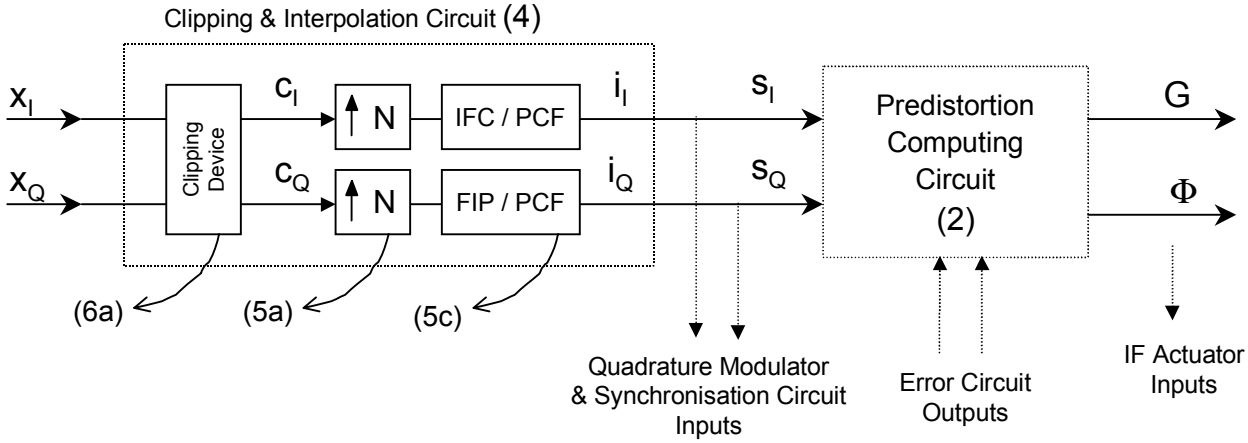


Fig. 2(b)

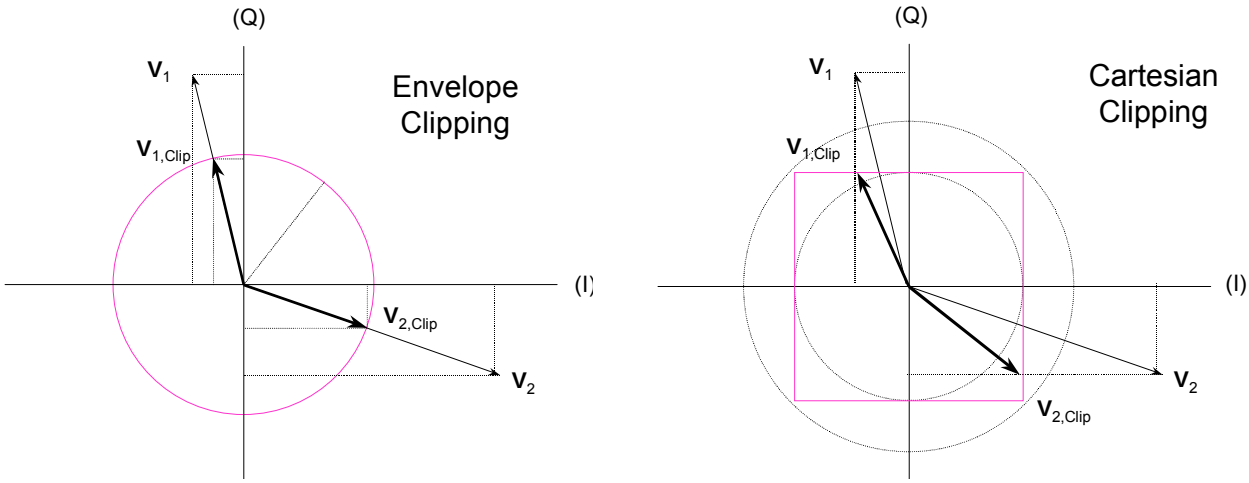


Fig.3 (a) Envelope Clipping; (b) Cartesian Clipping

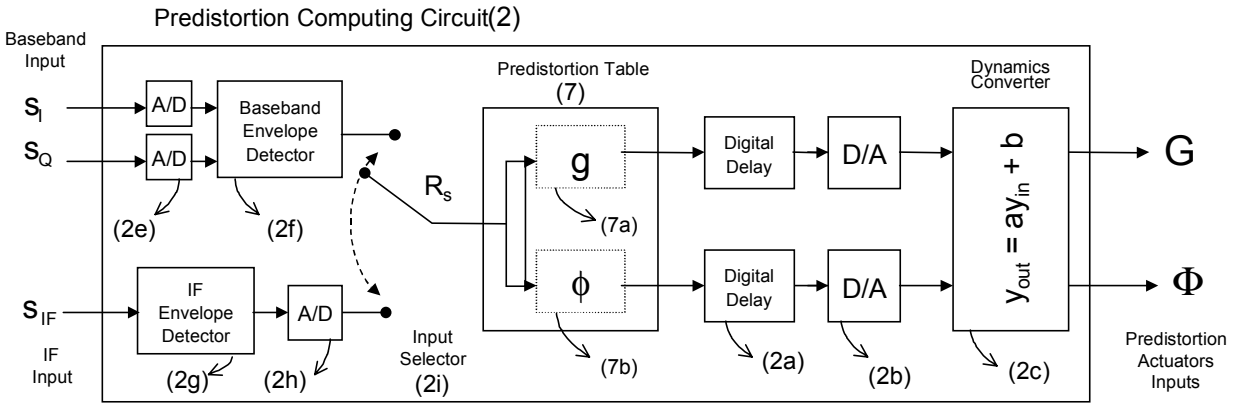


Fig.4

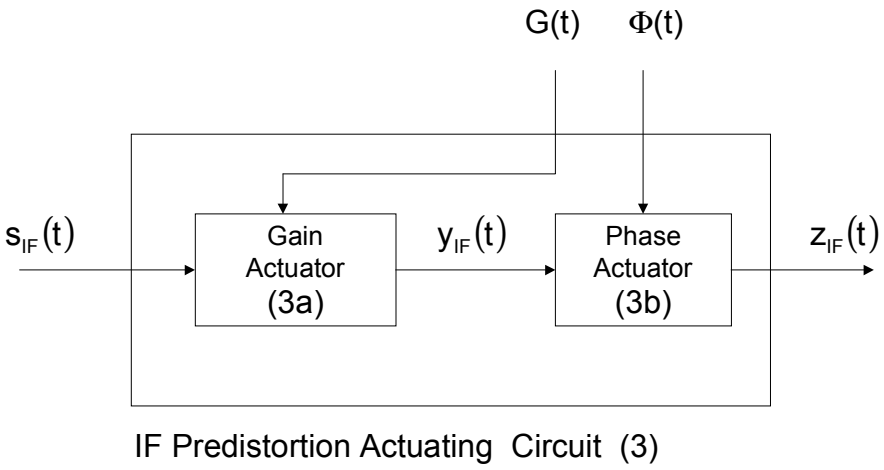
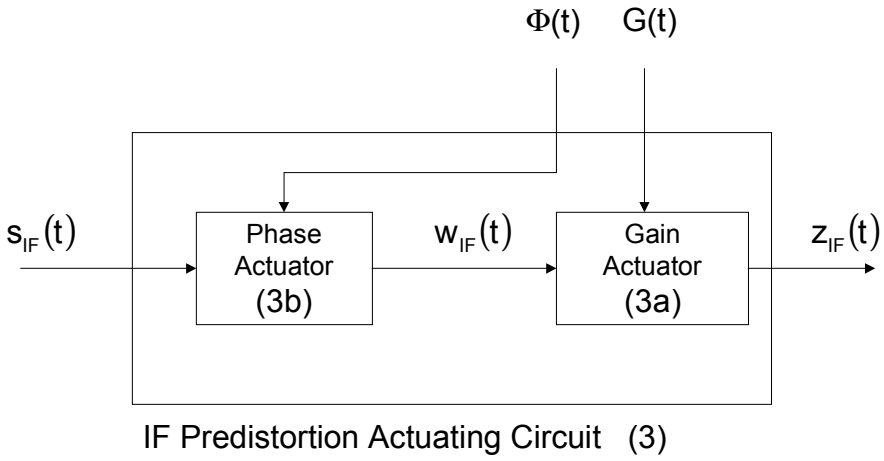
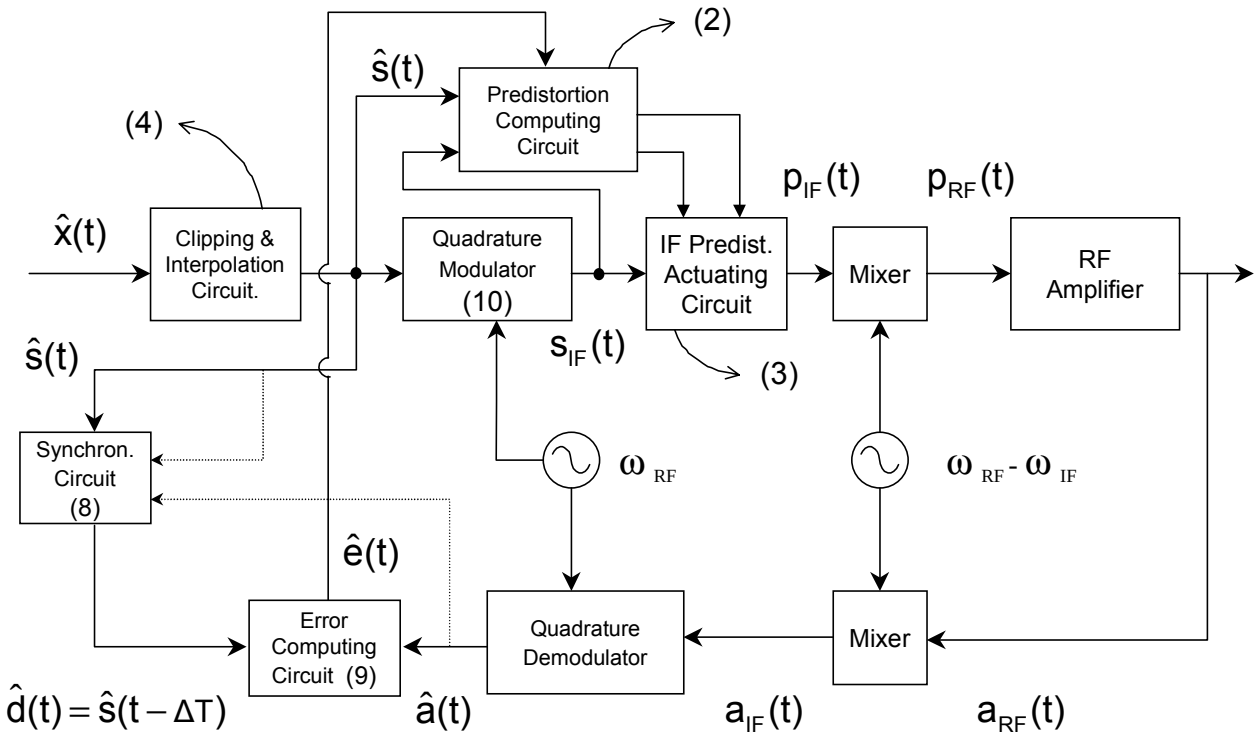


Fig. 5(a)



IF Predistortion Actuating Circuit (3)

Fig. 5(b)



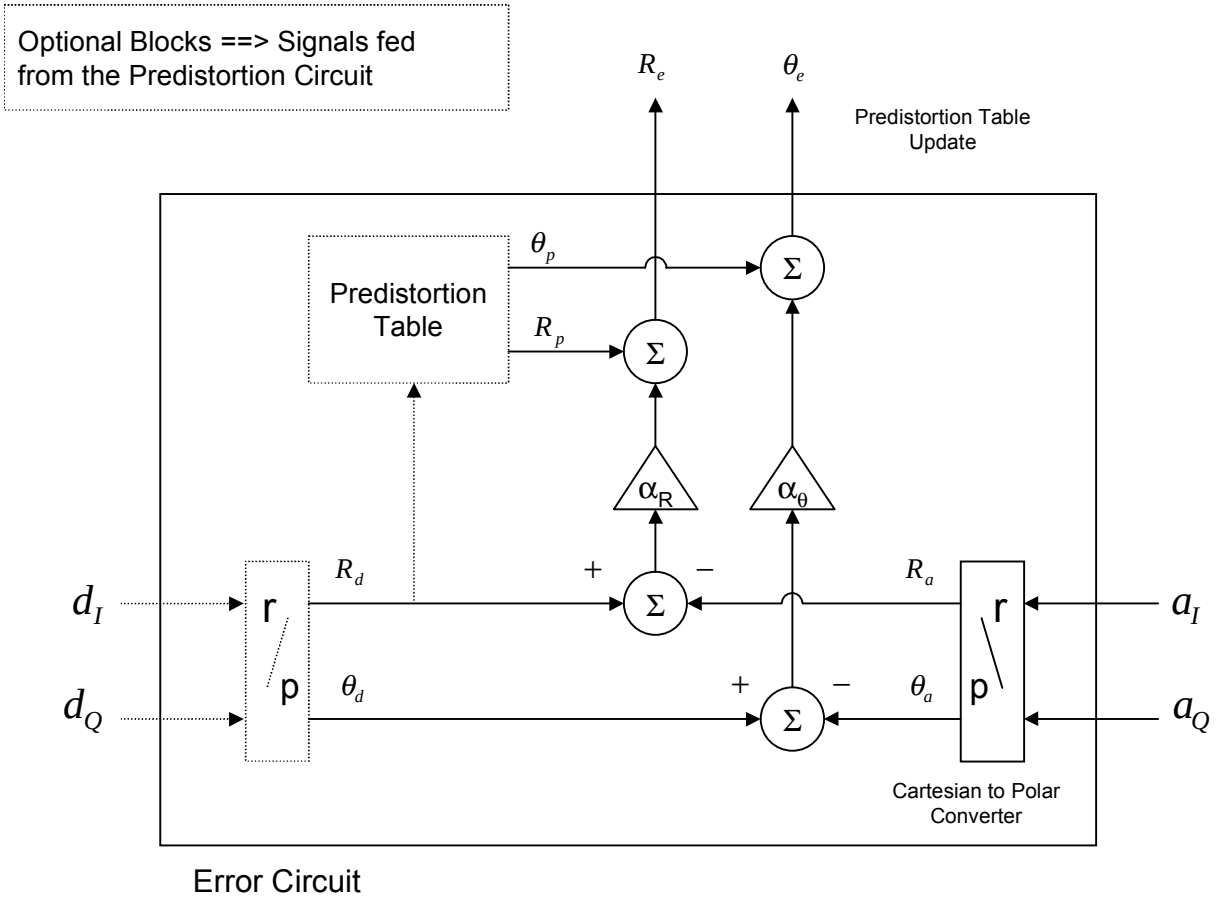

Optional Blocks ==> Signals fed from the Predistortion Circuit
R_e
θ_e
Predistortion Table Update
Predistortion Table
θ_p
R_p
Σ
α_R
α_θ
R_d
R_a
d_I
d_Q
r
p
θ_d
θ_a
a_I
a_Q
Cartesian to Polar Converter
Error Circuit

Fig.6

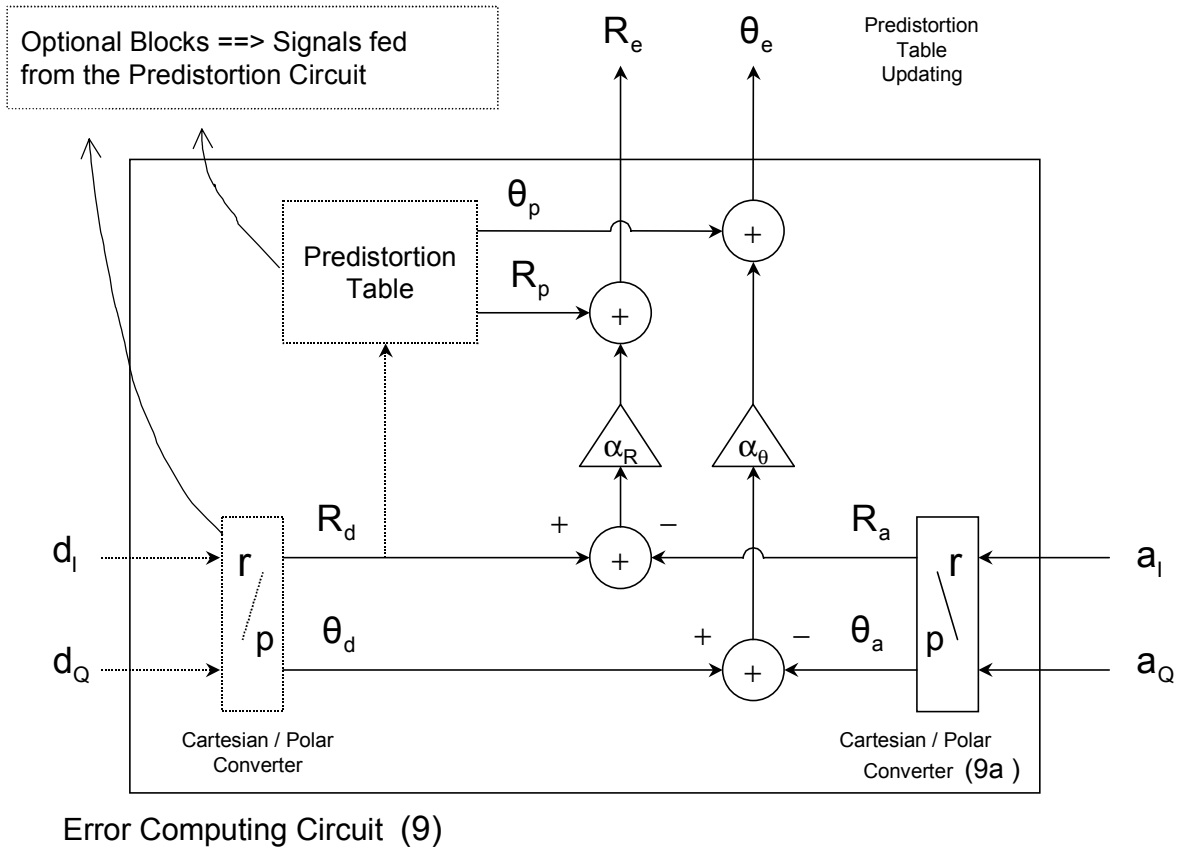

Optional Blocks ==> Signals fed from the Predistortion Circuit
R_e
θ_e
Predistortion Table Updating
Predistortion Table
θ_p
R_p
+
α_R
α_θ
R_d
R_a
d_I
d_Q
r
p
θ_d
θ_a
a_I
a_Q
Cartesian / Polar Converter
Cartesian / Polar Converter (9a)
Error Computing Circuit (9)

Fig. 7